Spartan-6 & Virtex-6 FPGA Connectivity Kit FAQ

April 04, 2011

Getting Started

1. ***Where can I purchase a kit?***

   A: You can purchase your Spartan-6 and Virtex-6 FPGA Connectivity kits online at:

   Spartan-6 FPGA Connectivity Kit: http://www.xilinx.com/s6connkit

   Virtex-6 FPGA Connectivity Kit: http://www.xilinx.com/v6connkit

   or contact your local Xilinx Distributor or Representative at:
   http://www.xilinx.com/company/sales/ww_disti.htm

3. ***When will I get my kit?***

   A: Order entry for the Spartan-6 FPGA Connectivity Kit and the Virtex-6 FPGA Connectivity Kit is now open. The lead times are posted on the kit ordering pages.

   The ISE Design Suite Embedded Edition software included in the kit is available for you to download immediately upon purchasing the kit. You will be sent an email with instructions to help you to register and generate a software license when you place your order. See FAQ answer to “How do I register and install my software?” below for instructions.

   For the Spartan-6 FPGA Connectivity Kit only, the full version of the Northwest Logic DMA IP core is also included as part of the kit purchase and is available for you to download immediately upon purchasing the kit. You will be sent an email with instructions to help you to register and generate a IP license when you place your order. See FAQ answer to “How do I register and install the Northwest Logic’s DMA Controller IP included with the Spartan-6 FPGA Connectivity Kit?” below for instructions.

   The documentation and reference designs for the Spartan-6 FPGA Connectivity Kit are available for download now at:
   http://www.xilinx.com/products/boards/s6conn/reference_designs.htm

   The documentation and reference designs for the Virtex-6 FPGA Connectivity Kit are available for download now at:
   http://www.xilinx.com/products/boards/v6conn/reference_designs.htm

General Kit Questions

4. What is included in the Spartan-6 FPGA Connectivity Kit and Virtex-6 FPGA Connectivity Kit?

A: These kits includes the following Items

Key Features	***Virtex-6 Connectivity Kit*** ***DK-V6-CONN-G*** ***DK-V6-CONN-G-J***	***Spartan-6 Connectivity Kit*** ***DK-S6-CONN-G*** ***DK-S6-CONN-G-J***
Silicon:	**XC6VLX240T-FF1156-1C**	**XC6SLX45T-FG484C-3C**
Base Board:	ML605	SP605
Daughter Card	FMC-Connectivity Daughter card (CX4,SMA,SATA)	-
Loopback Module	CX4 Loopback Module	-
FPGA Programming Cable & Power Supply	✓	✓
I/O, DATA Cables	4 SMA cables 1 Ethernet cable 1 USB cable 1 SATA cable 1 SATA loopback cable	4 SMA cables 1 Ethernet cable 1 USB cable
ISE Design Suite: Embedded Edition	13.1	13.1
Connectivity Targeted Reference Design	PCIe–10GDMA–DDR3–XAUI (now available with **AXI4 Interconnect support**)	PCIe–DMA–DDR3–GbE (now available with **AXI4 Interconnect support**)
NORTHWEST LOGIC PCIe Packet DMA IP core (delivered as Encrypted NETLIST)	Evaluation only, Hardware Timeout Version	Full Production Version
Physical Media (USB Stick)	✓	✓
What Design on Platform Flash (V6) / SPIx4 Flash (S6)?	PCIe – 10GDMA – DDR3 - XAUI	PCIe – DMA – DDR3 –GbE
What Design on SystemACE?	IBERT2.0 Design (3.125Gbps)	IBERT2.0 Design (2.5Gbps)

Key Features	*Virtex-6 Connectivity Kit* ***DK-V6-CONN-G*** ***DK-V6-CONN-G-J***	*Spartan-6 Connectivity Kit* ***DK-S6-CONN-G*** ***DK-S6-CONN-G-J***
Documentation: **Welcome Letter, Hardware Setup Guide & Getting Started Guide, Connectivity Targeted Reference Design User Guide**	✓	✓
Board Design Files / Gerber Files / Layout and Schematic files	✓	✓
Fedora 10 Live CD Linux Operating System	✓	✓
Support	Customers can get support through the normal Xilinx channels including Xilinx Hotline support	

5. What expansion ports are available on CONNECTIVITY Kits?

A: Both the Spartan-6 and Virtex-6 CONNECTIVITY kits include FPGA Mezzanine Connector (FMC) expansion slots.

The Spartan-6 FPGA Connectivity Kit provides the FMC-LowPinCount (LPC) connector. The Virtex-6 FPGA Connectivity Kit provides both the FMC-LPC and the FMC-HighPinCount (HPC) connector. As detailed in the table above, the Virtex-6 FPGA Connectivity Kit ships with the FMC Connectivity Daughter Card which provides access to the XAUI, SATA and SMA connectivity.

Additional FMC-LPC and FMC-HPC daughter cards are available from multiple board vendors.

6. What is the FMC expansion connector and what can I connect to it?

A: FPGA Mezzanine Card (FMC) is an expansion card interface format developed by a consortium of companies ranging from FPGA vendors to end users to provide a standard mezzanine card form factor, connectors and modular interface to an FPGA located on a base board, also called a carrier card. Decoupling the I/O interfaces from the FPGA in this manner simplifies the design of the I/O interfacing modules while maximizing carrier card reuse. Please find more information at http://www.xilinx.com/fmc

7. How do I get a copy of the FMC specification?

A: FPGA Mezzanine Card (FMC) is a VITA specification and is available on VITA's website at: https://www.vita.com/online-store.html.

8. ***Do the Xilinx CONNECTIVITY Kits come with Loopback cables / modules to aid design debug?***

   A: Yes – both Connectivity kits include 4 SMA cables. This will enable designers to loopback their transceiver designs through the SMA connector and these SMA cables and simplify design development and debug.

   Additionally, the Virtex-6 FPGA Connectivity kit also ships with

   - SATA loopback cable to enable loopback of the SATA connectors on the FMC Connectivity Daughter Card
   - CX4 loopback module to enable loopback of the CX4 connector on the FMC Connectivity Daughter card

9. ***I have already bought an Evaluation kit – Spartan-6 SP605 Evaluation kit or Virtex-6 ML605 Evaluation kit. Since the board used in the Connectivity Kits is the same, can I upgrade without having to buy the new kit?***

   A: Yes – you can upgrade to the Spartan-6 FPGA Connectivity kit if you have already purchased the Spartan-6 SP605 Evaluation kit AND you can upgrade to the Virtex-6 FPGA Connectivity kit if you have already purchased the Virtex-6 ML605 Evaluation kit.

   Detailed instructions on this upgrade are available at each of the Connectivity Kit webpages: http://www.xilinx.com/s6connkit and http://www.xilinx.com/v6connkit. If you need any more clarifications, please contact your local Xilinx FAE or sales.

10. ***Why is the Spartan-6 Connectivity Targeted Reference Design a PCIe-DMA-DDR3-GbE reference design?***

    A: The connectivity targeted reference design is a design framework that provides key elements to simplify and accelerate system design development. It is a modular and scalable building block architecture that promotes and encourages design re-use.

    The Spartan-6 Connectivity Targeted Reference Design is a PCIe-DMA-DDR3-GbE reference design. Customers can use this design as is in their application, or replace / modify the GbE interface to support other serial protocols like Serial RapidIO, Aurora, etc. The PCIe protocol implementation also provides bandwidth flexibility through support of multiple lane-width configurations like – x1,x4,Gen1 implementations as well.

    Through this design framework, customers can even modify the memory interfaces to support different memory interfaces as well like – DDR, DDR2, DDR3, LPDDR and others that are supported by the Memory Controller Blocks and the Xilinx MIG controller for the Spartan-6 FPGA.

    This inherent flexibility of the connectivity targeted reference design will enable the customers to quickly adapt the framework to suit their application needs.

    The Spartan-6 Connectivity Targeted Reference Design is a PCIe-DMA-DDR3-GbE reference design because of multiple reasons:

    PCIe is the most common I/O interface and protocol that a Xilinx customer is designing with in an FPGA. Also GbE is also the other most common media interface that is currently being designed with using multiple flavors. The GbE interface flavors supported in the Spartan-6 Connectivity Targeted Reference Design are GMII (through an on-board Marvel PHY) and SFP (Small Form-Factor Pluggable) through the Xilinx GTP transceiver running at 1.25Gbps industry standard.

    In addition, since most PCIe devices are memory mapped and data exchange happens by transferring data from local memory to system memory. To speed up the data exchange between the system memory and the local memory and to maintain efficiency of the PCIe link utilization, a DMA engine is needed. Also to enable faster accesses to the local on-board memory, DDR3 interfacing is a must. The Connectivity Targeted

Reference Design further simplifies this by implementing a Virtual FIFO memory controller around the built-in Memory Controller Block and providing this as a source file for the customer to modify. This design also provides a good example to highlight both this unique value of the Xilinx FPGA as well providing a good venue for teaching CONNECTIVITY design techniques – clocking, reset, design optimization scenarios, etc.

Also this design showcases the capability of the built-in block for PCIe as a x1Gen1 Endpoint (GTP Transceiver running at 2.5Gbps). Also through the GbE - SFP interface, we have another GTP transceivers running at 1.25 Gbps and the Memory Controller Block interfacing to a local memory through parallel I/O implementing DDR3 IOs running 16-bit @ 400MHz. There are multiple 62.5MHz clock domains supported in the design. So using the Connectivity Targeted Reference Design, a true system implementation can be demonstrated to the customer.

Pl. read the Connectivity Whitepaper at http://www.xilinx.com/connectivity.htm for details on the Connectivity Targeted Reference Design and the use-models.

11. Where can I find the design details for the Spartan-6 Connectivity Targeted Reference Design (PCIe-DMA-DDR3-GbE reference design)?

A: The Spartan-6 Connectivity Targeted Reference Design User Guide contains all the design details – I/O performance, Memory performance, FPGA Resource Utilization. Also provided are details on the optimizations that might be applicable to your design development goals.

Pl. visit the Spartan-6 Connectivity Kit website: http://www.xilinx.com/s6connkit

The complete design deliverables for the Spartan-6 Connectivity Targeted Reference Design can be downloaded as a zip file from http://www.xilinx.com/products/boards/s6conn/reference_designs.htm

12. Why is the Virtex-6 Connectivity Targeted Reference Design a PCIe-10GDMA-DDR3-XAUI reference design?

A: The connectivity targeted reference design is a design framework that provides key elements to simplify and accelerate system design development. It is a modular and scalable building block architecture that promotes and encourages design re-use.

The Virtex-6 Connectivity Targeted Reference Design is a PCIe-10GDMA-DDR3-XAUI reference design. Customers can use this design as is in their application, or replace / modify the XAUI interface to support other serial protocols like RXAUI, Serial RapidIO, Aurora, etc. The PCIe protocol implementation also provides bandwidth flexibility through support of multiple lane-width configurations like – x1, x4, x8 Gen1/Gen2 implementations.

Through this design framework, customers can even modify the memory interfaces to support different memory interfaces as well like – DDR, DDR2, DDR3, LPDDR and others that are supported by the Xilinx MIG controller for the Virtex-6 FPGA.

This inherent flexibility of the connectivity targeted reference design will enable the customers to quickly adapt the framework to suit their application needs.

The reason the Virtex-6 Connectivity Targeted Reference Design is a PCIe-10GDMA-DDR3-XAUI reference design is because of multiple reasons:

PCIe is the most common I/O interface and protocol that a Xilinx customer is designing with in an FPGA. Also XAUI is the most common backplane industry standard. In addition, since most PCIe devices are memory mapped and data exchange happens by transferring data from local memory to system memory. To speed up the data exchange between the system memory and the local memory and to maintain efficiency of the PCIe link utilization, a DMA engine is needed. Also to enable faster accesses to the local on-

board memory, DDR3 interfacing is a must. The Connectivity Targeted Reference Design further simplifies this by implementing a Virtual FIFO memory controller and providing this as a source file for the customer to modify. This design also provides a good example to highlight both this unique value of the Xilinx FPGA as well providing a good venue for teaching CONNECTIVITY design techniques – clocking, reset, design optimization scenarios, etc.

Also this design showcases the capability of the built-in block for PCIe as either the x4Gen2 Endpoint (4 GTX Transceivers running at 5.0 Gbps) or a x8Gen1 Endpoint (8 GTX transceivers running at 2.5Gbps) configuration. Also through the XAUI interface, we have 4 GTX transceivers running at 3.125 Gbps and the parallel I/O implementing DDR3 IOs running 64-bit @ 400MHz. There are multiple clock domains in the design supporting, 250MHz, 200MHz,156.25MHz,clock domains. So using the Connectivity Targeted Reference Design a true system implementation can be demonstrated to the customer.

Pl. read the Connectivity Whitepaper at http://www.xilinx.com/connectivity.htm for details on the Connectivity Targeted Reference Design and the use-models

13. Where can I find the design details for the Virtex-6 Connectivity Targeted Reference Design (PCIe-10GDMA-DDR3-XAUI reference design)?

A: The Virtex-6 Connectivity Targeted Reference Design User Guide contains all the design details – I/O performance, Memory performance, FPGA Resource Utilization. Also provided are details on the optimizations that might be applicable to your design development goals.

Pl. visit the Virtex-6 Connectivity Kit website: http://www.xilinx.com/v6connkit

The complete design deliverables for the Virtex-6 Connectivity Targeted Reference Design can be downloaded as a zip file from http://www.xilinx.com/products/boards/v6conn/reference_designs.htm

14. What IP interfaces are supported for the Connectivity Targeted Reference Designs?

A: Available now for **IDS 13.1** is Spartan-6 and Virtex-6 Connectivity Targeted Reference Designs supporting **AXI4 Interconnect Standard for designs targeting production silicon** only: Spartan-6 XC6SLX45T-FG484C-3C and Virtex-6: XC6VLX240T-FF1156-1C respectively.

The Spartan-6 Connectivity Targeted Reference Design – PCIe to GbE bridge includes:

a. GTP transceivers
b. Endpoint Block for PCIe, **supporting AXI4 Interconnect standard**
c. AXI-MIG Memory Controller Block supporting DDR/DDR2/DDR3 and LPDDR, **supporting AXI4 Interconnect standard**
d. Bus Mastering PCIe Packet DMA engine from Northwest Logic, **supporting AXI4 Interconnect standard** (optimized for Spartan-6 FPGA)
e. AXI Ethernet (Tri-Mode Ethernet MAC), **supporting AXI4 Interconnect standard**

The Virtex-6 Connectivity Targeted Reference Design – PCIe to XAUI bridge includes:

a. GTX transceivers
b. Endpoint Block for PCIe, **supporting AXI4 Interconnect standard**
c. Bus Mastering PCIe Packet DMA engine from Northwest Logic, **supporting AXI4 Interconnect standard** (optimized for Virtex-6 FPGA)

d. Xilinx 10 Gigabit Attachment Unit Interface (XAUI) Logicore IP

In addition, for customers still planning to use the supported legacy interfaces (Local Link, PLBv46, MIG-Native Interface) or the CES silicon, the Targeted Reference Designs are available to support these design preferences as well.

Pl. visit the following links for all details:

Spartan-6 Connectivity Targeted Reference Design:
http://www.xilinx.com/products/boards/s6conn/reference_designs.htm

Virtex-6 Connectivity Targeted Reference Design:
http://www.xilinx.com/products/boards/v6conn/reference_designs.htm

15. What is the DMA Controller included in the Spartan-6 FPGA Connectivity kit?

A: The DMA Controller IP included in the Spartan-6 FPGA Connectivity kit is a node-locked license of a FULL seat of the Production Netlist of Northwest Logic PCIe Packet DMA IP Core. This 32-bit DMA Controller IP core is optimized for the Spartan-6 FPGA architecture and can be targeted to any Spartan-6 FPGA.

The DMA Controller design deliverables can be accessed by / through:

1. Buying the Spartan-6 FPGA Connectivity kit. The files included in the USB memory stick are:
    a. Simulation Model
    b. Hardware Evaluation Netlist (time-limited to 12 hours)
    c. Production Netlist files are also included on the USB stick. However, the entitlement to the FULL production netlist is fulfilled only through the OMS licensing system. Customer will be sent an email on kit purchase with specific instructions to download their license files associated with the product. The license file is necessary and required step to unlock these production netlist files available on the USB stick.
        i. The license for the DMA Controller IP from NORTHWEST LOGIC is a Single-seat, Node-locked license.
        ii. For the DMA Controller IP included in the Spartan-6 FPGA Connectivity kit, this purchase also entitles the customer to all associated updates for the lifetime of the Spartan-6 FPGA Connectivity Kit. When the Spartan-6 FPGA Connectivity Kit is obsolete, the customer will be expected to contact Northwest Logic directly to extend the licensing, maintenance, support and upgrades for the DMA Controller IP
2. Web download: www.xilinx.com/s6connkit.
    a. Simulation Model
    b. Hardware Evaluation Netlist (time-limited to 12 hours)

16. What is the DMA Controller included in the Virtex-6 FPGA Connectivity kit?

A: The DMA Controller included in the Virtex-6 FPGA Connectivity kit is an evaluation version of the Northwest Logic PCIe Packet DMA IP Core. This 64-bit DMA IP core is optimized for the Virtex-6 FPGA architecture.

These DMA design deliverables can be accessed by / through:

1. Buying the Virtex-6 FPGA Connectivity kit. The files included in the USB memory stick are:
   a. Simulation Model
   b. Hardware Evaluation Netlist (time-limited to 12 hours)
2. Web download: www.xilinx.com/v6connkit.
   a. Simulation Model
   b. Hardware Evaluation Netlist (time-limited to 12 hours)

In addition, orders for the full production version of the Northwest Logic PCIe Packet DMA IP core can be placed here – http://www.nwlogic.com/packetdma

17. What version of Xilinx IP is supported in the Connectivity Targeted Reference Designs?

A: The Connectivity Targeted Reference Designs currently support ISE Design Suite 13.1: Embedded edition software. The Xilinx IP available and delivered with this version of ISE Design Suite is supported.

18. Is there a software driver provided for the Connectivity Targeted Reference Designs that include PCIe? If so, what OS is supported?

A: The Connectivity Targeted Reference Design deliverables also include software device drivers and a performance & status monitor application / GUI as well. This will enable to evaluate the system performance using the Connectivity Targeted Reference Design.

Currently the device drivers support Linux OS: Fedora 10 Live. Windows support for the device drivers will be provided in the very near future.

The Device Driver source files are also provided enabling you to modify the software architecture to fit your application needs.

Pl. visit the Spartan-6 Connectivity Kit website: http://www.xilinx.com/s6connkit or the Virtex-6 Connectivity Kit website: http://www.xilinx.com/v6connkit for more details to download the complete design deliverables through the zip file, including the software device driver source code.

19. What are the Targeted Reference Design Deliverables?

A: The Connectivity Targeted Reference Design is available through the respective Spartan-6 and Virtex-6 FPGA Connectivity Kits. The designs are also made available online through the respective Connectivity Kit webpages. The Targeted Reference Design deliverables include the following:

1. Design source and IP files: supporting Verilog HDL
   a. Top-level system integration RTL source files
   b. Xilinx CORE Generator™ technology for dedicated blocks and LogiCORE IP
   c. Third-party IP core deliverables and license management
2. Simulation environment: supporting Modelsim simulator
   a. Testbench and BFMs
   b. Scripts based simulation
3. Implementation environment: supporting XST and ISE 13.1 design flow
   a. FPGA/board constraint files
   b. Complete steps and parameters for design synthesis

c. MAP, place and route, and timing closure analysis
d. Automated scripts

4. Software deliverables: supporting Linux OS (Fedora 10 Live OS)
   a. Device driver source files
   b. Scripts to build and attach the software driver to the hardware board
   c. Performance & status monitor application and GUI
5. Documentation:
   a. Hardware Setup Guide
   b. Getting Started Guide
   c. Connectivity targeted reference design user guide

Software Related Questions

20. What is ISE Design Suite Embedded, S6LX45T or V6 LX240T Device Locked, Edition?

A: ISE Embedded Edition, device locked to S6LX45T (included in the Spartan-6 FPGA Connectivity kit) or the ISE Embedded Edition, device locked to V6LX240T (included in the Virtex-6 FPGA Connectivity kit) design software is the industry's fully featured FPGA design solution for Linux, Windows XP, and Windows Vista. This is a full feature software build, but it will only generate a bit stream for the specified devices only. To target other Xilinx devices, you will need to buy a full ISE Embedded Edition License.

This software provides a complete suite of RTL design and implementation tools for FPGA development including HDL synthesis and simulation, implementation, device fitting, and JTAG programming in addition to the Embedded Development Kit (EDK). Only the place and route environment is device locked to the specified devices only. The EDK can be used with a full seat of place and route to target all Xilinx devices.

21. How do I register and install my software?

A: The Xilinx Virtex-6 and Spartan-6 Connectivity Kits, entitle the ISE Design Suite: Embedded Edition software. The software can be installed from the DVD provided with the kit. The latest version can also be downloaded from http://www.xilinx.com/support/download/index.htm.

You can also follow the instructions found here:
http://www.xilinx.com/support/download/index.htm

If you log in with the Email address that was included in the purchase order, then you will already have an account created for you. If not, then you will need to register a new account.

The Spartan-6 FPGA Connectivity Kit comes with "entitlement" to a seat of the ISE Embedded, S6LX45T Device Locked Edition software and all associated updates for a one-year period, or as specified in your purchase order, if different.
The Virtex-6 FPGA Connectivity Kit comes with "entitlement" to a seat of the ISE Embedded, V6LX240T Device Locked Edition software and all associated updates for a one-year period, or as specified in your purchase order, if different.

A software voucher is included with each Xilinx Spartan-6 or Virtex-6 Connectivity Kit. The voucher contains the code that is used to create a device-locked software license for the ISE software.

Please visit the Xilinx software registration and entitlement site to follow detailed instructions: http://www.xilinx.com/getlicense

22. Why is ISE Design Suite: Embedded Device Locked Edition included with the Connectivity Kits?

A: The ISE Design Suite: Embedded Edition allows the customer to use the XPS-LL-TEMAC (Tri Mode Ethernet MAC) IP core from the EDK IP portfolio.

In future releases of these Connectivity kits, the connectivity targeted reference designs might be enhanced to include embedded processing performing system control and status functions. This also allows customers who have purchased the Connectivity kits to download the reference designs for the embedded kits without added expense and use the infrastructure provided in these reference designs to develop complete systems running on the FPGA.

23. How do I register and install the Northwest Logic's DMA Controller IP included with the Spartan-6 FPGA Connectivity Kit?

A: The Spartan-6 FPGA Connectivity Kit comes with "entitlement" to ONE FULL seat of the Northwest Logic's x1 Packet DMA IP core – Node Locked License and all associated updates for a one-year period, or as specified in your purchase order, if different.

A software voucher is included with each Spartan-6 FPGA Connectivity Kit. The voucher contains the code that is used to create a node-locked license for the Northwest Logic's x1 Packet DMA IP core.

Please visit the Xilinx software & IP registration and entitlement site: http://www.xilinx.com/getproduct

If you log in with the Email address that was included in the purchase order, then you will already have an account created for you. If not, then you will need to register a new account.

Generate a License: Under the "Create New License" tab, enter the code from the voucher and Click "Reedem Now" The software & IP represented by the voucher code is added to the product table and is selected (checked) for licensing "Spartan-6 FPGA Connectivity Kit, NWL x1 Packet DMA Back End Core".

Note: Laptop users may want to select your Hard Disk ID or Wireless Ethernet card HostID. If you are going to select an Ethernet adaptor, it is best to select your wireless card. If you select your Docking Station HostID, you will only be licensed when you are docked. Also, many direct RJ45 Ethernet connections on Laptop computers are powered down when not plugged into the network, so if you are not connected with a cable, you may also find that you are not licensed.

After you have selected a HostID, click the "Generate Node Locked License" button. This will generate your license in the "Manage Licenses" tab as well as email you a copy of the license.

Installing the IP Node-locked License:
These steps will copy your license file to the appropriate default directory (the .Xilinx directory under your home drive – typically C: for Windows).

1. Save the license file to your desktop or some other folder on your computer
2. Run the Xilinx License Configuration Manager
   Windows: Run 'Manage Xilinx Licenses' from Xilinx ISE Design Suite 12

Linux: Type 'xlcm' in a command-line window

3. Select the 'Manage Xilinx Licenses' tab and click on the 'Copy License…' button
4. Browse to the downloaded license file and click 'Open'

24. How can a customer get started with the Spartan-6 FPGA Connectivity Kit or the Virtex-6 FPGA Connectivity Kit?

A: Included with every kit is a HARDWARE SETUP GUIDE and GETTING STARTED GUIDE. Customers are expected to read and follow instructions in the Hardware Setup Guide and bring up the Connectivity Targeted Reference Design Demonstrations included with each of the Connectivity kits. In addition, if they want to evaluate the system performance and modify design parameters and check the design flow, they should go through the details in the Getting Started Guide. If they are interested in additional details, they should refer to the Spartan-6 Connectivity Targeted Reference Design User Guide or the Virtex-6 Connectivity Targeted Reference Design User Guide which outlines more steps to get them familiarized with the design.

All these Setup and User Guides are included as printed and/or electronic versions in the Spartan-6 FPGA Connectivity Kit or the Virtex-6 FPGA Connectivity Kit.

25. Will the Spartan-6 and Virtex-6 Connectivity Targeted Reference Designs be supported for the next version of the ISE Design Suite?

A: The Spartan-6 and Virtex-6 Connectivity Targeted Reference Designs are delivered with the Xilinx Spartan-6 and Virtex-6 FPGA Connectivity Kits respectively.

In addition, these Targeted Reference Designs will be maintained and updated for every ISE Design Suite release until the lifetime of the Connectivity Kits – typical kit lifetime is ~2years,

26. How can a customer get support on the Spartan-6 FPGA Connectivity Kit or the Virtex-6 FPGA Connectivity Kit?

A: Customers can get support through the normal Xilinx channels including Xilinx Hotline support.

Getting More Information

27. What other Connectivity Targeted Reference Designs are available?

A: Xilinx has plans to provide more Connectivity Reference Designs for both the Spartan-6 and Virtex-6 FPGA Connectivity Kits. Pl. contact your Xilinx FAE for more details and detailed roadmap information for the Spartan-6 and Virtex-6 Connectivity Targeted Reference Designs will be provided.

28. Where do I get more information?

A: Please visit the Xilinx Connectivity webpage at http://www.xilinx.com/connectivity.htm